

1 **COMPUTER SYSTEM BUS INTERFACE AND CONTROL METHOD THEREFOR**

2

3 **FIELD OF THE INVENTION**

4 The present invention relates to a computer system with SCSI
5 (Small Computer System Interface), a bus interface and a
6 control method therefor, and in particular to an effective
7 technique for use in bus control when a contention of SCSI
8 device IDs occurs.

9

10 **BACKGROUND ART**

11 SCSI (Small Computer System Interface) is a well-known
12 standard I/O bus. Standards have been established for bus
13 widths of 8 bits and 16 bits that provide a maximum data
14 transfer rate of 160 MB/sec. According to the standard for
15 the 8 bit bus width, up to eight device IDs (#0 to #7) can
16 be assigned while, according to the standard for the 16 bit
17 bus width, up to 16 device IDs (#0 to #15) can be assigned.
18 A host computer must also be assigned a device ID, which is
19 typically #7. A variety of devices, including hard disk
20 drives, CD-ROMs and scanners, can be connected to a SCSI
 bus.

1 Because of a demand for high extensibility in a computing
2 system, there has been a great demand for connecting
3 multiple storage devices to the system. Particularly, in an
4 environment wherein multimedia data are frequently handled,
5 a lot of voluminous image data may be recorded. Considering
6 use for servers, it is desired to implement data storage of
7 around 500 GB, preferably at a low price. Since many SCSI
8 compatible hard disk drives have been developed, and SCSI is
9 readily extended by using a daisy chain, a mass storage
10 system can be constituted by connecting multiple hard disk
11 drives to a SCSI bus.

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13 Generally, multiple hard disk drives are housed in a hard
14 disk enclosure. Such a hard disk enclosure is provided with
15 a host computer interface card and a service processor for
16 controlling the hard disk drives. Since the host computer
17 and the service processor are also connected to the SCSI
18 bus, they are assigned unique device IDs, respectively. For
19 example, for a 16 bit bus width, #7 is assigned to the host
20 computer and #15 is assigned to the service processor.

Thus, for such a hard disk enclosure, excluding the device

1 IDs assigned to the host computer and the service processor,
2 fourteen device IDs are available so that up to fourteen
3 hard disk drives can be connected to the SCSI bus.

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5 However, there may be a need to connect an additional host
6 computer to enhance redundancy, taking system reliability
7 into consideration. The second host computer may be
8 connected through the interface card like the first host
9 computer, and assigned a device ID #6, for example. In such
10 a case, if a hard disk drive mounted in a hard disk
11 enclosure has already been assigned the same device ID #6, a
12 device ID contention would occur. The device ID contention,
13 if occurred, would cause a failure, e.g., data to be written
14 to a hard disk drive by the second host computer are lost,
15 or data recorded on the hard disk drive #6 are lost.

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1 **SUMMARY OF THE INVENTION**

2 It is, therefore, an object of the present invention to
3 prevent a failure such as loss or corruption of data from
4 occurring when a device ID contention occurs.

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6 An overview of the present invention will now be given.

7 According to the present invention, when a second, or
8 subsequent, host computer contends with another device that
9 is connected to a SCSI bus for the use of a device ID, a
10 reset signal (RST) is transmitted to a SCSI control bus
11 input of the contending device. Determination for a
12 contention is made depending on whether or not a terminal
13 power of the second or subsequent host computer is active.
14 In such a manner, the contending device can be disconnected
15 from the SCSI bus by inputting the reset signal to the
16 device when the terminal power of the contending host
17 computer is active (the computer has been powered on and is
18 running). By disconnecting the device, the contention can
19 be eliminated and a failure such as loss of data can be
20 prevented.

1 The reset signal to be input to the contending device may be
2 generated by inputting the terminal powers of the host
3 computers to an AND gate, and inputting the output of the
4 AND gate and the original SCSI reset signal to an OR gate,
5 wherein the output signal of the OR gate is employed as the
6 reset signal. During the operation of a host computer that
7 has the same device ID as a specific device, the reset
8 signal to the device is constantly generated. But when the
9 host computer having the same device ID is not active, the
10 specific device can be controlled by the original SCSI reset
11 signal.

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13 Further, a latch circuit may be provided between the output
14 of the AND gate and the input of the OR gate so that once
15 the reset signal is input to the contending device, it can
16 be continuously applied regardless of the state of the
17 terminal power. This causes the contending device to be
18 maintained in the reset state even if, for example, the
19 terminal power of the host computer becomes inactive due to
20 momentary power outage. Therefore, it is possible to
prevent unexpected situations from occurring, e.g., loss of

1 data due to the momentary power outage which may cause the
2 contending device to be released from the reset state.

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4 Further, if SCSI operates with low-voltage differential
5 signals, a low-voltage differential signal from the SCSI bus
6 is input to the OR gate after it is converted to a TTL level
7 signal, and the output of the OR gate is input to a device
8 after it is converted to a low-voltage differential signal.

9 The device may be a hard disk drive.

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11 **BRIEF DESCRIPTION OF THE DRAWINGS**

12 Fig. 1 is a block diagram showing an example of a computer
13 system according to one embodiment of the present invention.

14 Fig. 2 illustrates a connection of a SCSI bus with slots in
15 an enclosure.

16 Fig. 3 is a detailed block diagram illustrating a reset
17 signal control circuit. Fig. 4 is a block diagram showing
18 another example of a computer system according to the
19 embodiment.

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1 **PREFERRED EMBODIMENTS**

2 The preferred embodiments of the present invention will now
3 be described in detail with reference to the accompanying
4 drawings. It should be noted, however, that the present
5 invention can be variously modified, and should not be limited
6 to the embodiments. The same reference numerals are used
7 throughout the description of the embodiments to denote
8 corresponding or identical components.

9
10 Fig. 1 is a block diagram illustrating an example of a
11 computer system according to the embodiment of the present
12 invention. The computer system in this embodiment comprises
13 a host computer Host0, a host computer Host1, an enclosure
14 2, and interface cards 3 and 4.

15
16 The first host computer Host0 has a device ID of, for
17 example, #7 and is connected to a SCSI bus of the enclosure
18 2 via the interface card 3. The second host computer Host1
19 has a device ID of, for example, #6 and is connected to the
20 SCSI bus of the enclosure 2 via the interface card 4.

Although the device ID (#7) having the highest priority is

1 assigned to the host computer Host0, and the device ID (#6)
2 having the second highest priority is assigned to the host
3 computer Host1 in this embodiment, other device IDs may be
4 assigned to the host computers.

5
6 The enclosure 2 includes fourteen slots 5-0 to 5-6, 5-8 to
7 5-14 to which hard disk drives can be attached,
8 respectively. The number of each slot (i.e., "n" in 5-n)
9 denotes a device ID number to be assigned. In this
10 embodiment, the device ID (#6) of the host computer Host1
11 contends with the device ID (#6) of the device (hard disk
12 drive) attached to the slot 5-6. The contention is resolved
13 as described later. If the host computer Host1 is not used
14 and the device ID #6 is not reserved therefor, the device ID
15 #6 may be assigned to another device (a hard disk drive in
16 this case). Therefore, a maximum storage capacity can be
17 obtained by connecting the maximum number of hard disk
18 drives to the SCSI bus. Each slot is connected by a SCSI
19 bus 6 which is terminated by terminators 7.

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1 The interface cards 3 and 4 include service processors 8 and
2 9 for the enclosure 2, respectively. The service processors
3 8 and 9 are responsible for overall control of the enclosure
4 2 to, for example, determine whether a hard disk drive is
5 attached to a slot, monitor and control temperature and
6 power of the hard disk drives. Such service functions need
7 not be performed by both of the service processors 8 and 9.

8 When the service processor 8, for example, is performing
9 the service functions, the service processor 9 may operate
10 as a slave under the control of the service processor 8.

11 The service processors 8 and 9 are connected to SCSI buses
12 10 in the respective interface cards 3 and 4, and device ID
13 #15 is assigned to the service processor 8.

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15 Repeaters 11 may be provided in the respective interface
16 cards 3 and 4. The repeater 11 serves as a driver for
17 maintaining signal levels above a predetermined level when a
18 longer SCSI bus is used. SCSI buses 19 of the interface
19 cards 3 and 4 are terminated by terminators 20, and
20 connected to the host computers Host0 and Host1,
respectively.

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2 Table 1 shows a list of device IDs assigned in the above
3 manner.

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5 [Table 1]

6	Device ID	Device
7	ID#0	Hard disk drive #0
8	ID#1	Hard disk drive #1
9	ID#2	Hard disk drive #2
10	ID#3	Hard disk drive #3
11	ID#4	Hard disk drive #4
12	ID#5	Hard disk drive #5
13	ID#6	Host1 or hard disk drive #6
14	ID#7	Host0
15	ID#8	Hard disk drive #8
16	ID#9	Hard disk drive #9
17	ID#10	Hard disk drive #10
18	ID#11	Hard disk drive #11
19	ID#12	Hard disk drive #12
20	ID#13	Hard disk drive #13
	ID#14	Hard disk drive #14
	ID#15	Enclosure service processor

Fig. 2 illustrates connections of the SCSI bus 6 of the enclosure 2 with the slots 5-0 to 5-6, 5-8 to 5-14. The SCSI bus includes 16 data bus lines and some control lines.

The control lines include +RST and -RST lines for providing a low-voltage differential signal. In this embodiment, each signal transmitted is assumed to be a low-voltage

1 differential signal; however, a high-voltage differential
2 signal or a negative logic TTL level signal may also be
3 employed. Although not shown in the drawing, it should be
4 noted that each of the data bus lines #0 to #15 in this
5 embodiment actually consists of plus (+) and minus (-) lines
6 for transmission of differential signals.

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8 The slot 5-0 is connected to the control lines including
9 +RST and -RST lines (the other control lines are not shown)
10 and to the data bus consisting of 16 data lines, and is
11 associated with the data line #0 for a device ID.
12 Therefore, a device attached to the slot 5-0 is assigned a
13 device ID #0. Similar connection and association are
14 implemented for the other slots. That is, the slots 5-1 to
15 5-5 are associated with the data lines #1 to #5,
16 respectively, and the slots 5-8 to 5-14 are associated with
17 the data lines #8 to #14, respectively. The numbers of the
18 associated data lines are assigned as device IDs for the
19 devices attached to the respective slots. Such device ID
20 assignment by association with data lines has been well
known in the art.

1 Although all the 16 data lines are actually connected to the
2 slots 5-n (n is an integer of 0 to 14), only the connection
3 of the data line with the associated slot is shown in Fig. 2
4 in order to clearly indicate the association therebetween,
5 but the connection of the 16 data lines with each slot is
6 not shown.

7

8 In this embodiment, a reset signal control circuit 12 is
9 inserted between the reset signal input of the slot 5-6 and
10 the reset lines (+RST and -RST lines) of the control lines.
11 The reset signal control circuit 12 receives terminal power
12 signals from the host computers Host0 and Host1 to control
13 the device attached to the slot 5-6 in accordance with the
14 terminal power states.

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16 Fig. 3 is a detailed block diagram illustrating the reset
17 signal control circuit 12, which includes a low-voltage
18 differential signal receiver 13, an AND gate 14, a latch
19 circuit 15, an OR gate 16 and a low-voltage differential
20 signal driver 17.

1 The low-voltage differential signal receiver 13 converts a
2 low-voltage differential signal on the SCSI bus to a TTL
3 level signal. The AND gate 14 receives as inputs the
4 terminal power signals from the host computers Host0 and
5 Host1, and the latch circuit 15 latches the output voltage
6 of the AND gate 14. The outputs of the low-voltage
7 differential signal receiver 13 and the latch circuit 15 are
8 input to the OR gate 16, and the low-voltage differential
9 signal driver 17 converts the output of the OR gate 16 to a
10 low-voltage differential signal.

11
12 In the reset signal control circuit 12, when the terminal
13 power signals from the host computers Host0 and Host1 are
14 both active, i.e., the two host computers are running, the
15 output of the AND gate 14 (latch circuit 15) and, hence, the
16 output of the OR gate 16 goes high, and a reset signal is
17 applied to the device having the device ID #6. As a result,
18 the device having the device ID #6 is disconnected from the
19 SCSI bus. The disconnected device is treated as though it
20 does not exist on the SCSI bus. In this fashion, the device
ID contention between the host computer Host1 and the device

1 attached to the slot 5-6 is avoided. When the host computer
2 Host1 is not active, a reset signal from the SCSI bus is
3 transmitted via the OR gate 16 to the device so that the
4 device having the device ID #6 can be operated normally.

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6 The latch circuit 15 is provided to maintain the reset state
7 of the device once the active state of the host computer
8 Host1 is detected to cause the device to be reset. Even if
9 the terminal power goes low due to a failure such as
10 momentary halt of the computer system, the output of the
11 latch circuit 15 is kept high so that the reset state of the
12 device is not altered. This prevents the reset state from
13 being canceled due to the momentary halt or the like, and
14 avoids unexpected situation such as data loss or corruption.
15 In this case, a reset operation may be performed by powering
16 off the enclosure 2.

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18 According to the computer system of the present embodiments,
19 wherein a plurality of host computers are connected via the
20 SCSI bus to a plurality of devices, a device ID contention
can be avoided while maintaining a capability of connecting

1 the maximum number of devices. Therefore, the present
2 invention provides an environment wherein a mass storage
3 system is controlled by a plurality of host computers via
4 SCSI.

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6 The present invention has been specifically described with
7 respect to the preferred embodiments; however, the present
8 invention is not limited to the above embodiments, and can
9 be variously modified without departing from the scope of
10 the invention.

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12 For example, although it has been assumed in the above
13 embodiments that the contention of device ID #6 occurs, the
14 present invention may be applied for a contention of another
15 device ID. Further, by providing a plurality of reset
16 signal control circuits 12, the present invention may also
17 be applied to a case in which a plurality of device IDs
18 contend.

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20 In addition, the present invention may also be applied to
other devices such as CD-ROM, scanner, etc. in place of or

1 in addition to the hard disk drive used in the above
2 embodiments.

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4 The reset signal control circuit 12, which has performed the
5 required functions by a combination of AND and OR gates, may
6 employ other logical gates to perform the same functions.

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8 Furthermore, although the low-voltage differential signal
9 has been used in the above embodiments, a high-voltage
10 differential signal or a TTL level negative logical signal
11 may be used instead. In such a case, an appropriate
12 receiver and driver suitable for these signals and
13 corresponding to the low-voltage differential signal
14 receiver 13 and the low-voltage differential signal driver
15 17 may be adopted.

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17 Moreover, a bus width of 16 bits has been employed; however,
18 the present invention may also be applied in the same manner
19 for a bus width of 8 bits.

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1 Furthermore, the SCSI bus 6 of the enclosure 2 in the above
2 embodiments may be divided at a repeater 18 as shown in Fig.
3 4. Terminators 21 are provided at both ends of the repeater
4 18. When the repeater 18 is disconnected, the slots on the
5 left are separated from the slots on the right, and the host
6 computers Host0 and Host1 can control the respective devices
7 independently of each other. When the repeater 18 is

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1 connected, the system can be controlled in the same manner
2 as in the above embodiments.

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4 According to the present invention disclosed herein, a
5 failure such as data loss or corruption can be prevented
6 when a device ID contention occurs between devices
7 interconnected by a SCSI bus.

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9 What is claimed is:

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